AMENDED CLAIM SET:

1. (currently amended) A DRAM, comprising:

at least one primary sense amplifier, wherein the at least one primary sense amplifier has single ended sensing, has data storage and data write-back capability, ~~and has~~ wherein the write-back comprises at least ~~two amplification stages; and~~ one passtransistor:

a plurality of storage cells and a plurality of bitlines, with a single ended bitline structure, wherein one storage cell of the plurality of storage cells and the at least one primary sense amplifier are connected by one single bitline of the plurality of ~~bitlines.~~ bitlines; and

a plurality of secondary sense amplifiers and a plurality of global bitlines, with a single ended global bitline structure, wherein the at least one primary sense amplifier and one secondary sense amplifier of the plurality of secondary sense amplifiers are connected by one single global bitline of the plurality of global bitlines.

2. (canceled)

3. (original) The DRAM of claim 2, wherein the DRAM further comprises a small voltage swing design.

4. (previously presented) The DRAM of claim 2, wherein at least one of the plurality of secondary sense amplifiers comprise at least two amplification stages.

5. (previously presented) The DRAM of claim 2, wherein the at least one primary sense amplifier is being capable to decouple from the one single global bitline.

6. (original) The DRAM of claim 1, wherein the at least one primary sense amplifier comprises MOS devices, and wherein at least one of the MOS devices has a customized threshold.

7. (original) The DRAM of claim 6, wherein the customized threshold is dynamically adjusted.

8. (original) The DRAM of claim 1, wherein the DRAM is an embedded DRAM.

9. (previously presented) A DRAM, comprising:

a single ended bitline structure, wherein the DRAM has bitlines;

a single ended global bitline structure, wherein the DRAM has global bitlines;

a plurality of primary sense amplifiers operationally engaging the bitlines and the global bitlines, wherein the primary sense amplifiers have data storage and data write-back capability, and wherein the primary sense amplifiers are being capable to decouple

from the global bitlines;

a full-wordline I/O structure comprising a reduced address space, wherein the reduced address space has no column address; wherein essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense amplifiers, wherein the DRAM has memory cells and wordlines; and

a pipelined architecture, wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and wherein the pipelined architecture comprise synchronized operations of the single ended bitline structure, of said single ended global bitline structure, of the primary sense amplifiers, and of the full-wordline I/O structure.

10. (canceled)

11. (previously presented) The DRAM of claim 9, wherein a Read command and a subsequent WriteBack command are executed in differing cycles of the cycles.

12. (previously presented) The DRAM of claim 9, wherein a Read command and a subsequent WriteBack command are executed in a single one of the cycles.

13. (canceled)

14. (previously presented) The DRAM of claim 9, wherein a Read command and a Write command are executed simultaneously in a single one of the cycles.

15. (original) The DRAM of claim 9, wherein a size of the DRAM can be increased in a modular manner.

16. (original) The DRAM of claim 15, wherein the modular manner increase comprise an I/O increase.

17. (original) The DRAM of claim 15, wherein the modular manner increase comprise a banking increase.

18. (original) The DRAM of claim 9, wherein the DRAM further comprises a small voltage swing design.

19. (canceled)

20. (original) The DRAM of claim 9, wherein the DRAM is an embedded DRAM.

21. (previously presented) A processor, comprising:

at least one embedded DRAM macro, wherein the at least one embedded DRAM

macro is further comprising:

a single ended bitline structure, wherein the DRAM has bitlines;

a single ended global bitline structure, wherein the DRAM has global bitlines;

a plurality of primary sense amplifiers operationally engaging the bitlines and the global bitlines, wherein the primary sense amplifiers have data storage and data write-back capability, and wherein the primary sense amplifiers are being capable to decouple from the global bitlines;

a full-wordline I/O structure comprising a reduced address space, wherein the reduced address space has no column address; wherein essentially all memory cell that are simultaneously turned on by any one wordline are being operated on by associated sense amplifiers of the primary sense amplifiers, wherein the DRAM has memory cells and wordlines; and

a pipelined architecture, wherein the DRAM is functioning in cycles and in each of the cycles an operation can be initiated, and wherein the pipelined architecture comprise synchronized operations of the single ended bitline structure, said single ended global bitline structure, the primary sense amplifiers, and the full-wordline I/O structure.

22. (canceled)

23. (original) The processor of claim 21, wherein the DRAM further comprises a small voltage swing design.